UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,515	07/16/2003	Kelvin S. Vartti	RA 5487	8491

27516 7590 11/28/2005

UNISYS CORPORATION
MS 4773
PO BOX 64942
ST. PAUL, MN 55164-0942

EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/620,515	VARTTI ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7/16/2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following are quotations of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 3-4, and 6-10 are rejected under U.S.C. 102(b) as being anticipated by Luan et al. (US Patent 5,911,149).

Claim 1. A memory System, comprising: *(Abstract, line 2 – Discloses a memory system)*

- a first storage device; *(Figure 1A, number 104 – Shows a storage device)*
- at least one additional storage device; *(Figure 1A, number 107 – Shows an additional storage device)*
- a control storage device to store a programmable indicator identifying the manner in which the first and the at least one additional storage device are to be referenced; and *(Column 4, lines 44-48 – Disclose a system controller which is coupled to each memory configuration controller (control storage device))*
- a control circuit coupled to the first storage device, the at least one additional storage device, and the control storage device, *(Column 4, lines 49-54 – State that there is a memory configuration controller that is coupled to the shared memory, associated memory, and system controller)*
- the control circuit to receive a request for data, *(Column 4, lines 52-54 – Disclose a signal received to the memory configuration controller)*

- wherein the data may be stored within at least one of the first or the at least one additional storage device, and in response thereto, to initiate at least one of a first reference to the first storage device and a second reference to the at least one additional storage device in a manner controlled by the state of the programmable indicator. *(Column 4, lines 56-60)*

Claim 3. The system of Claim 1, wherein if the programmable indicator is in a first state, the second reference is issued only if the first reference is not capable of completing the request. *(Column 4, lines 59-60 – Disclose that the memory configuration controller couples the memory I/O port to the HPB, pending that the there is no coupling to the SMB)*

Claim 4. The system of Claim 3, wherein if the programmable indicator is in a second state, the second reference is issued regardless of whether the second reference is required to complete the request. *(Column 5, Table 2 – Shows that whether or not the "Select" is a "1" or a "0", the "OE" will be "1")*

Claim 6. The system of Claim 1, and further including mode switch logic to modify the state of the programmable indicator between the first state and the second state based on programmable criteria. *(Column 4, lines 56-67 – Disclose a mode select control signal and memory configuration controllers which modify the states)*

Claim 7. The system of Claim 6, wherein the control circuit receives multiple requests for data, (*Column 11, line 1 – States that there are configuration requests)*

- and wherein the mode switch logic includes a circuit to modify the state of the programmable indicator from the first state to the second state if at least a first predetermined number of the multiple requests requires the second reference to complete. *(Column 2, lines 33-45 – State that the programmable shared memory dynamically configures*

the memory during start up during a memory configuration request. In other words, the states are changed)

Claim 8. The system of Claim 7, wherein the mode switch logic includes a circuit to modify the state of the programmable indicator from the second state to the first state if a second predetermined number of the multiple requests does not require the second reference to complete. *(Column 2, lines 33-45 – State that the programmable shared memory dynamically configures the memory during start up during a memory configuration request. In other words, the states are changed)*

Claim 9. The system of Claim 8, wherein the mode switch logic includes a circuit that allows at least one of the first and the second predetermined numbers to be programmably selected. *(Column 2, line 42 – States that this is programmable architecture)*

Claim 10. The system of Claim 8, and further including a main memory coupled to the first storage device to issue the request to the control circuit. *(Column 9, lines 1-3 – State that the associated memory is coupled to the processor bus)*

3. Claims 12-20, and 22-32 are rejected under U.S.C. 102(b) as being anticipated by Baror (US Patent 5,627,992)

Claim 12. A memory system, comprising:

- first memory logic; *(Figure 3, number 305 – Shows Memory Address Logic)*
- at least one other memory; *(Figure 1, numbers 102 and 190 – Show a data cache and a memory respectively)*
- a storage device coupled to the first memory logic to store a programmable indicator identifying a mode of referencing the first memory logic and the at least one other memory; and *(Column 50, lines 36-67 – State that there is a control unit (which store the memory logic) coupled to the block status array (which is a plurality of storage*

locations), and the control unit is configured to store "a value indicative of a write-through write mode into said status field of a particular one of a plurality of storage locations)

- a control circuit coupled to the first memory logic and the at least one other memory, the control circuit to receive a request for data, and in response thereto, to retrieve the requested data from at least one of the first memory logic and the at least one other memory in a manner determined by the identified mode. *(Column 51, lines 57-67 and Column 52, lines 1-12 – State that there is a control circuit performs a write-through operation is response to a write hit to a particular cache block associated with a cache-block status field which indicates said copy-back state)*

Claim 13. The system of Claim 12, wherein the first memory logic includes at least one of a tag memory and a memory to store data. *(Column 5, lines 61-67)*

Claim 14. The system of Claim 12, wherein the control circuit includes a circuit to determine whether the programmable indicator is in a first predetermined state, and if so, to further determine whether the at last one other memory must be referenced to complete the request, and if not, to obtain the data from the first memory logic without reference to the at least one other memory. *(Column 51, lines 57-67 and Column 52, lines 1-18- State that there is a control circuit that is "configured to set said state of said cache block status flied to indicate said write-through write mode if said first input line conveys said write-through status, even if said TLB write policy field is set in said second TLB write policy field)*

Claim 15. The system of Claim 14, wherein the control circuit includes a circuit to initiate references to both the first memory logic and the at least one other memory if the at least one other memory must be referenced to complete the request. *(Column 54, lines 18-27 – State that the control circuit is configured to perform a write-through operation associated with a cache block status field, ands stores data in a particular cache data subsystem)*

Claim 16. The system of Claim 12, wherein the control circuit includes a circuit to determine whether the programmable indicator is in a second predetermined state, and if so, to initiate a reference to the first memory logic and the at least one other memory irrespective of whether a reference to the at least one other memory is necessary to complete the request. *(Column 52, lines 59-64 – State that if the TLB write policy field is in the second state, then the policy-pins are placed into the first state regardless)*

Claim 17. The system of Claim 12, wherein the control circuit includes a circuit to determine if the programmable indicator is in a third predetermined state indicating the first memory logic is unavailable for storing data, and if so, to initiate a reference to the at least one other memory without attempting to obtain the requested data from the first memory logic. *(Column 13, lines 7-13 – State that there is a third state that indicated the program mode during memory access. Also, the "ICU transfers the value presented on the processor bus to the memory bus")*

Claim 18. The system of Claim 12, wherein the first memory logic includes a shared cache, wherein the at least one other memory includes one or more dedicated caches, and further comprising at least one instruction processor coupled to the one or more dedicated caches. *(Column 7, lines 11-20)*

Claim 19. The system of Claim 12, and further comprising a main memory coupled to the first memory logic to issue the request for the data. *(Column 45, lines 40-42 – State that there is logic that should be capable of monitoring all main memory accesses)*

Claim 20. The memory system of Claim 12, and further including mode switch logic coupled to the storage device to automatically re-program the programmable indicator. *(Column 25, lines 24-37 – State that there is a method to switch between two caches for programming)*

Claim 22. A method for use in a data processing system having a first memory coupled to at least one other memory and a programmable storage device to identify a reference mode to control the manner in which data is

retrieved from at least one of the first memory and the at least one other memory, the method comprising: *(Column 50, lines 36-67 – State that there is a control unit (which store the memory logic) coupled to the block status array (which is a plurality of storage locations), and the control unit is configured to store "a value indicative of a write-through write mode into said status field of a particular one of a plurality of storage locations)*

a.) receiving a request for data; and *(Column 8, line 62 – Discloses a data request. Column 50, lines 44-45 – State that there is a first input configured to convey a first write-through status value)*

b.) initiating an operation to retrieve data from at least one of the first memory or the at least one other memory in a manner that is determined by the reference mode. *(Column 50, lines 48-50 – State that there is an operation for receiving the status value from the buffer)*

Claim 23. The method of Claim 22, wherein step b.) comprises:

- if the reference mode selects a first mode, determining whether the request can be completed without accessing the at least one other memory; *(Column 2, lines 42-44 – State that the cache block status field indicate whether or not the cache is shared or exclusive, thereby signifying whether or not other memories must be accessed)*
- and if the request can be completed without accessing the at least one other memory, obtaining the requested data from the first memory. (Column 2, lines 44-47 – State that the cache block status field controls which mode the control unit operates in)

Claim 24. The method of Claim 22, wherein step b.) comprises:

- if the reference Mode selects a first mode, determining whether the request can be completed without accessing the at least one other memory; *(Column 2, lines 42-44 – State that the cache block status field indicate whether or not the cache is shared or exclusive, thereby signifying whether or not other memories must be accessed)*

- and if the request cannot be completed without accessing the at least one other memory, initiating references to the first memory and the at least one other memory to complete the request.

Claim 25. The method of Claim 22, wherein if the reference mode selects a second mode, initiating a reference to the first memory and the at least one other memory irrespective of which of the first memory or the at least one other memory stores the data. *(Column 31, lines 22-30 – State that a first word is written into the cache during the second cycle and deals with the buffer)*

Claim 26. The method of Claim 22, wherein step b.) comprises:

- determining that the first memory is unavailable to store the requested data; *(Column 34, lines 42-44 – State that the requested data cannot be stored in the cache array)*
- and obtaining the requested data from the at least one other memory. *(Column 34, lines 32-39 – State that a variable or instruction may be fetched from a four word read buffer)*

Claim 27. The method of Claim 22, and further including modifying the reference mode based on conditions within the data processing system. *(Column 4, lines 64-67 – State that there is a "block modified relative to the main memory")*

Claim 28. The method of Claim 22, wherein the data processing system includes a main memory coupled to the first memory, *(Column 53, lines 44-45 – State that there is write buffer coupled to the storage array)*

- and wherein step a.) includes receiving a request for data from the main memory. *(Column 8, line 62 – Declares a data request)*

Claim 29. The method of Claim 22, wherein the at least one other memory includes multiple coupled memories, and wherein step b.) comprises *(Column 53, lines 44-45 – State that there is write buffer coupled to the storage array)*

- issuing a request for the requested data to the multiple coupled memories; *(Column 12, lines 33-34 – State that the ICU uses the signals as outputs)*

- and receiving the requested data from one of the multiple coupled memories. *(Column 12, lines 34-36 – State that the ICU uses the signals as inputs)*

Claim 30. A data processing system, comprising: *(Column 3, lines 35 – Discloses a RISC processing system)*

- main memory means for storing data; *(Column 3, lines 62-63 – A main memory is disclosed)*
- first cache means for storing a first sub-set of the data; second cache means for storing a second sub-set of the data; *(Column 3, line 40 – States that there are two ICUs (integrated cache units))*
- programmable storage means for storing one or more control signals to control the way in which data is retrieved from the first cache means and the second cache means; and *(Column 7, lines 59-64)*
- control means for receiving requests for data from the main memory, the control means further for initiating a reference to one or both of the first and second cache means based, at least in part, on the state of the one or more control signals. *(Column 51, lines 57-67 and Column 52, lines 1-12 – State that there is a control circuit performs a write-through operation is response to a write hit to a particular cache block associated with a cache-block status field which indicates said copy-back state)*

Claim 31. The system of Claim 30, and further including mode switch means for monitoring system conditions and automatically altering one or more of the control signals based on the system conditions. *(Column 25, lines 15-23 – State that the instruction can be "issued as part of the context switch procedure", which means that the cache configuration is reconfigured utilizing an easy method)*

Claim 32. The system of Claim 30, wherein the first cache means includes tag means for storing tag information describing the first sub-set of the data; *(Column 5, lines 61-65)*

- and wherein the control means includes means for initiating a reference to one or both of the first and 4 the second cache means based, at least in part, on tag information for the requested data. *(Column 5, lines 62-64 – State that "a cache tag is associated with each block, and it is stored in the cache array")*

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 2 and 5 are rejected under 35 U.S.C.103(a) as being unpatentable over Luan et al. as applied to claims 1 and 3-4 above.

Luan teaches the limitations of claims 1 and 3-4 for the reasons above.

Luan's invention differs from the claimed invention in that there is no specific reference to the order in which the references are issued in regards to the states.

Luan fails to teach claims 2 and 5, which respectively state "The system of Claim 1, wherein the first and the second references are issued in a time order that is controlled by the state of the programmable indicator", and "The system of Claim 4, wherein if the programmable indicator is in the second state, the second reference is issued before the first reference." However, stating that there is a sequence in which things must occur does not change the purpose or functionality of the claimed invention. Therefore, it would have been obvious to one of ordinary skill in the art to enable Luan's "Shared Memory" to have the indicator controlled by a time order and by changing state orders.

For further information, reference Ex parte Rubin , 128 USPQ 440 (Bd. App. 1959) (Prior art reference disclosing a process of making a laminated sheet wherein a base sheet is first coated with a metallic film and thereafter impregnated with a thermosetting material was held to render prima facie obvious claims directed to a process of making a laminated sheet by reversing the order of the prior art process steps.). See also In re Burhans, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) (selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results); In re Gibson, 39 F.2d 975, 5 USPQ 230 (CCPA 1930) (Selection of any order of mixing ingredients is prima facie obvious.).

6. Claim 11 is rejected under 35 U.S.C.103(a) as being unpatentable over Luan et al. as applied to claims 1, 6-8, and 10 above, further in view of Baror. (US Patent 5,627,992).

Luan teaches the limitations of claims 1, 6-8, and 10 or the reasons above.

Luan's invention differs from the claimed invention in that there is no specific reference to a memory map.

Luan fails to teach claim 11, which states "The system of Claim 10, wherein the request is requesting data associated with one or more incomplete memory coherency actions, and further comprising a request tracking circuit coupled to the control circuit to track the incomplete memory coherency actions, whereby the data is returned to the main memory only after all of the coherency actions are completed." However, Baror's invention discloses the following: "Ownership--This is a scheme to guarantee data consistency. The most current value of a variable is owned by one cache or the main memory. It is the responsibility of the owner to maintain the consistency of the variable. There are several ownership schemes which differ in the number of states that are attributed to a variable and the algorithms for ownership and state

transitions." (Column 7, lines 6-11). It would have been obvious to one of ordinary skill in the art, having the teachings of the "Shared Memory Apparatus" of Luan and Baror's "Integrated Cache Unit" before him at the time the invention was made, to allow cache coherency to occur by utilizing a tracking device, since cache coherency is vital for a system to run efficiently and without error.

7. Claims 21 is rejected under 35 U.S.C.103(a) as being unpatentable over Baror (US Patent 5,627,992) as applied to claims 12 and 20 above.

Baror teaches the limitations of claims 1 and 3-4 for the reasons above.

Baror's invention differs from the claimed invention in that there is no specific reference to the automating of the programming process.

Baror fails to teach claim 21, which respectively state "The memory system of Claim 20, wherein the mode switch logic includes a circuit to monitor conditions within the memory system, and to automatically re-program the programmable indicator based on the monitored conditions." However, Baror does state that "The Chip Select Mapping Register...specifies the address and the conditions for the ICU chip and its functions" (Column 17, lines 21-25)." Therefore, stating that the above is done automatically does not change the purpose or functionality of the claimed invention. Therefore, it would have been obvious to one of ordinary skill in the art to enable Baror's "Integrated Cache Unit" to automate the re-programming in order to make the whole programming process faster and more user-friendly.

For further information, reference Venner, 262 F.2d 91, 95, 120 USPQ 193, 194 (CCPA 1958) (Appellant argued that claims to a permanent mold casting apparatus for molding trunk

pistons were allowable over the prior art because the claimed invention combined "old permanent-mold structures together with a timer and solenoid which automatically actuates the known pressure valve system to release the inner core after a predetermined time has elapsed." The court held that broadly providing an automatic or mechanical means to replace a manual activity which accomplished the same result is not sufficient to distinguish over the prior art.).

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER